Digital Signal Termination

A Selection of Methods to Reduce Reflection and Improve Signal Integrity Along Digital Data Lines

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Signal Integrity and Reflections

A designer has many options to choose from in their effort to manage signal integrity in their digital systems. Different methods have different benefits and problems, though when chosen correctly, most applications will be adequately served with even the most simple methods.

The main objective of the designer in their effort to maintain signal integrity is to eliminate reflections. Just like water or sound waves, the travelling wavefront of a digital signal has a non-infinite speed, and when reflected off a change in environment, can cause constructive and destructive interference. Like a concrete pool wall is more dense than water and will reflect water waves, an increase in conductor impedance will reflect electrical waves. The same will happen with a decrease in impedance.

Reflection concerns are also increased with the physical distance that a signal must travel. If the signal only has to travel a very short distance with respect to the period of the digital signal, reflections will likely die down faster than the time it takes the load input to register a state change.

The typical solution for a designer to eliminate reflections is to use **termination**.

Termination Methods

Load Termination Resistor This, alongside source termination, is one of the most simple and commonly used termination methods. In this configuration, the designer will add a parallel resistor at the load input, reducing the impedance at the load.

Having termination at the one end of the signal's path will mean that very little will reflect from the load end, but reflections will still occur at the source end. In most cases this will not cause problems, but in the case of noise coupled onto the wire, this means noise will only be absorbed at one end and will reflect at the other.

Ideally it will be roughly matched to be around the characteristic impedance of the transmission line, though the designer must keep in mind that the resistance must not be so low as to significantly divide the voltage of the signal. To prevent this, the source impedance must be well known - or risk reducing the signal voltage so much that it is no longer reaching a defined high logic level, creating a different signal integrity problem.

Reducing the resistance of the load may also increase the EMC immunity of the particular signal line. Noise coupled onto the line will be more readily shunted away at the load, and unable to produce a significant voltage change.

Reducing the load impedance also has other pitfalls; having lower load resistance will increase steady state current along the data line, increasing power consumption of the device. Though it may not seem like much, many designers are on tight power and thermal budgets and everything counts.

Source Termination Resistor As mentioned above, source termination resistors are also very commonly used and very simple. Instead of placing a parallel resistor at the load, a series resistor is placed at the source, increasing the resistance to roughly match the characteristic impedance of the transmission line.

Like a load resistor, this means that reflections can still happen at one end of the wire, but still is unlikely to cause significant

problems.

The designer must be aware that reducing the source resistance will similarly divide the active logic level voltage of the signal, and must not add more source impedance than the characteristic impedance of the transmission line.

Source impedance has the benefit of reducing EMC emissions in a lot of cases, though it has the downside of being more susceptible to noise - poorer EMC immunity.

Load *and* Source Termination Combining the two above methods would reduce most downsides of either method, creating a more robust digital signal, but this is very often not necessary.

For the vast majority of cases, in both commercial and industrial applications, one of the first two methods will be perfectly adequate.

Load RC Termination In this method, the designer places a series resistor close to the load, with a capacitor to ground on the load side of the resistor.

The benefit of this over a simple load resistor is that in steady state logic level high, there is little current being shunted away once the capacitor is charged. The steady state power draw will be reduced, while maintaining a low impedance for the AC component of the signal.

The capacitor must be selected such that the RC timer created will still charge fast enough to maintain clean signal edges. The designer must have knowledge of the signal's clock frequency and the maximum acceptable rise or fall time of the load device. The capacitor should not be so large as to make the signal state transition too slow for the load device, but not so small as to ruin the reason for having it there in the first place.

The resistor can be selected in the same way as the simple parallel load resistor. This is because while the capacitor is charging

up, the AC component of the wavefront will approximately see the capacitor as a short to ground.

Source RC Termination In this method, the designer places a series resistor close to the source, with a capacitor to ground placed very close next to it on the load side of the resistor.

The created RC timer must still be considered with respect to the clock frequency of the signal and allowed rise and fall time.

The series resistor is selected in the same way as the simple series resistor termination. The AC component of the wavefront will see the capacitor as an approximate short to ground, so the resistor can be selected to be equal to the characteristic impedance of the transmission line.

This configuration should have the best EMC emissions performance.

When to Avoid Termination

Crystals Crystal clock and even crystal oscillator output lines are typically kept as short as possible, which should eliminate the need for termination. They should never be sent over long distances. This is because crystal resonance is strongly dependent on load impedance, and an oscillator signal should be kept as clean and robust as possible.

RF Applications RF impedance matching is much more frequency dependent, and often requires much more case-specific design. Tools like smith charts are often used in order to match an impedance transition to the characteristic impedance of a line. This is usually done with combinations of series and shunt capacitors and inductors. Resistors are less often used.